

FIG. 1

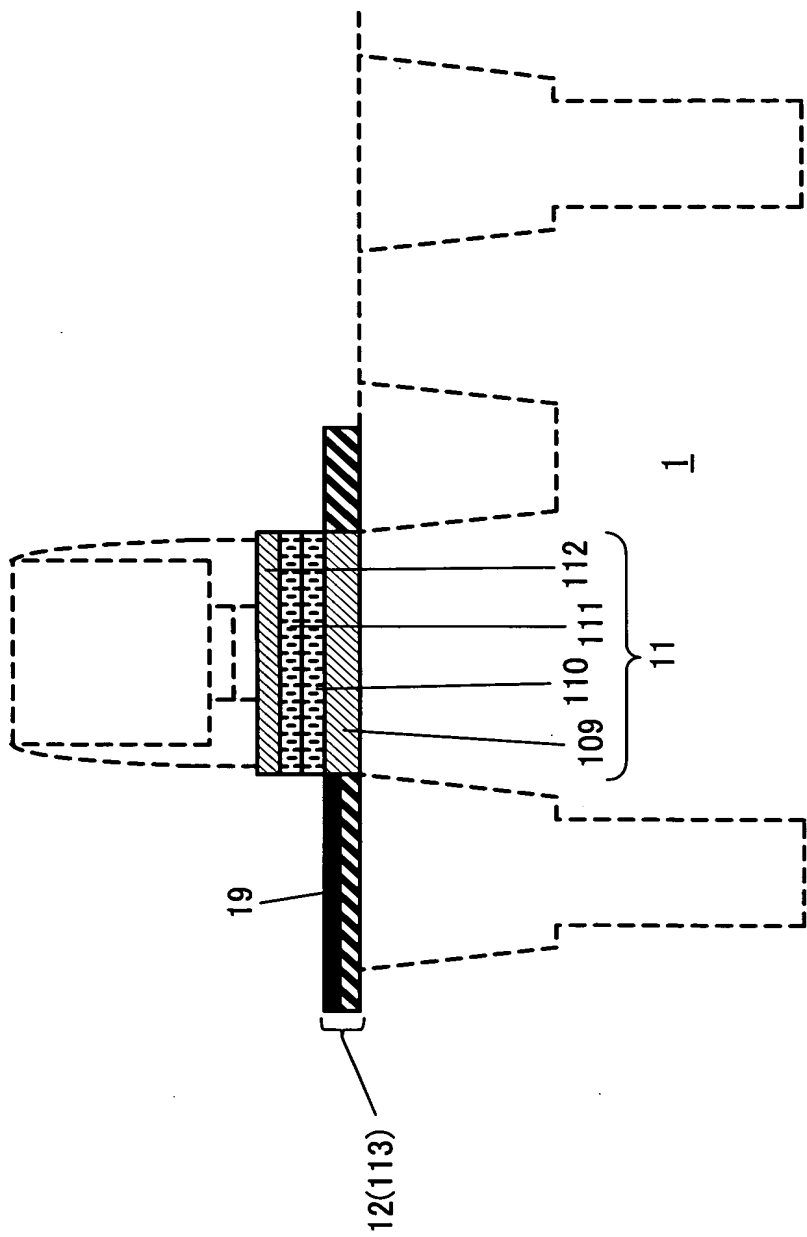
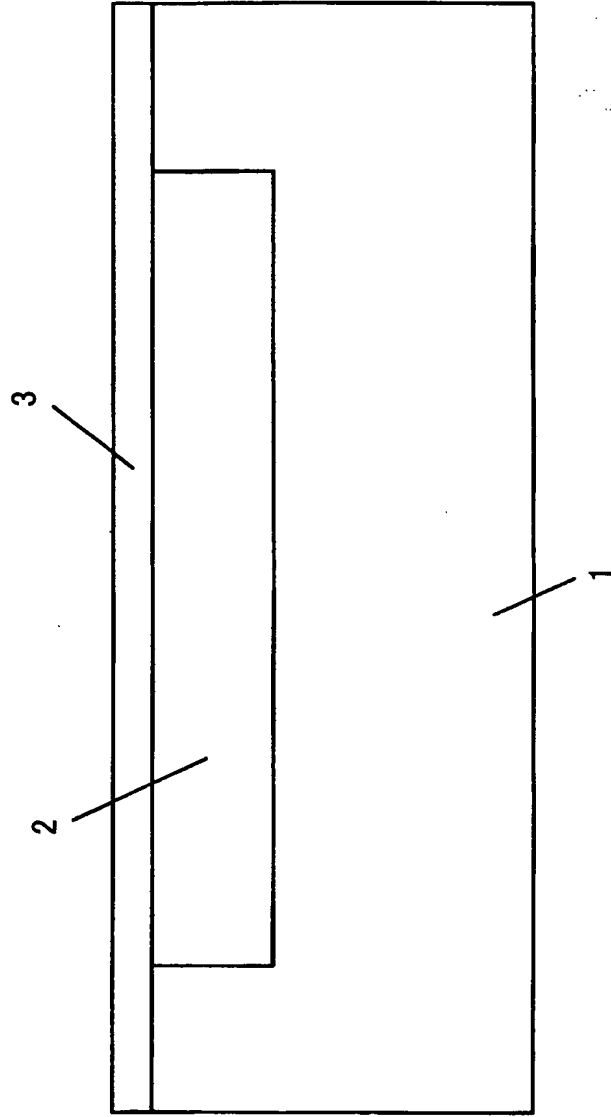


FIG. 2



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FIG. 3

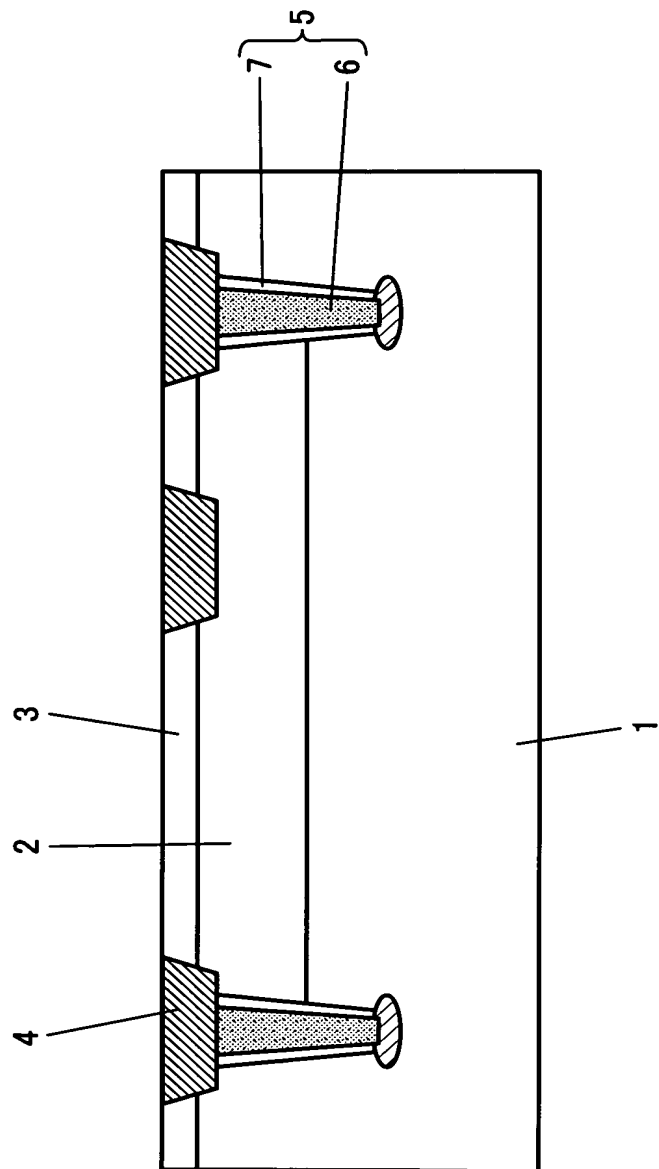
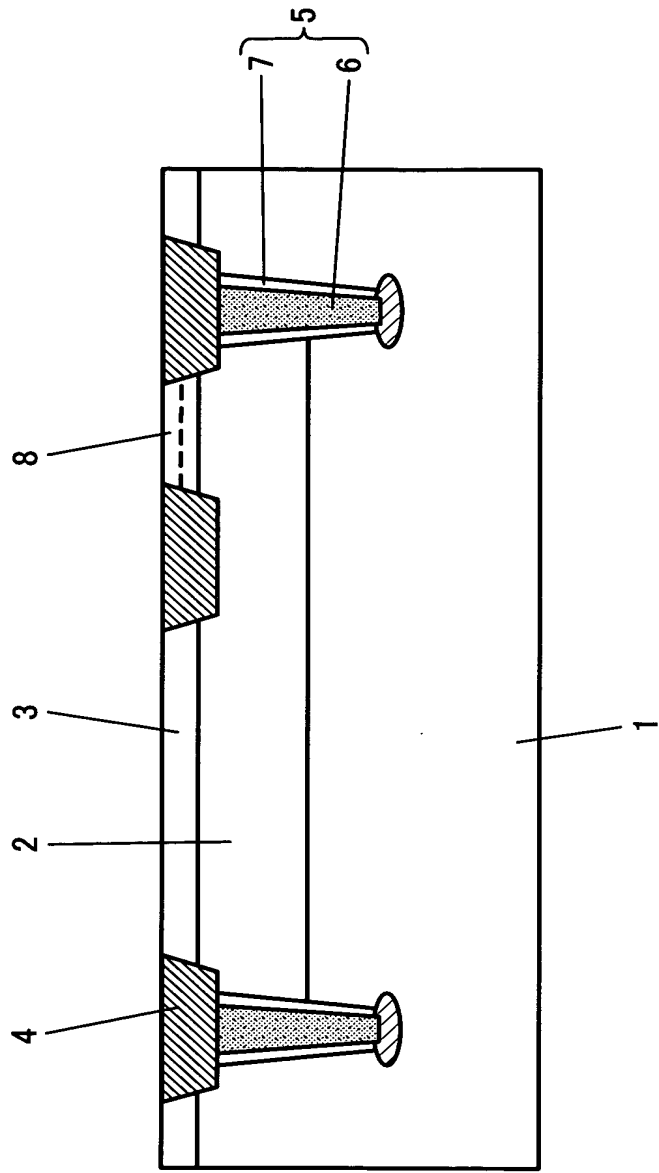
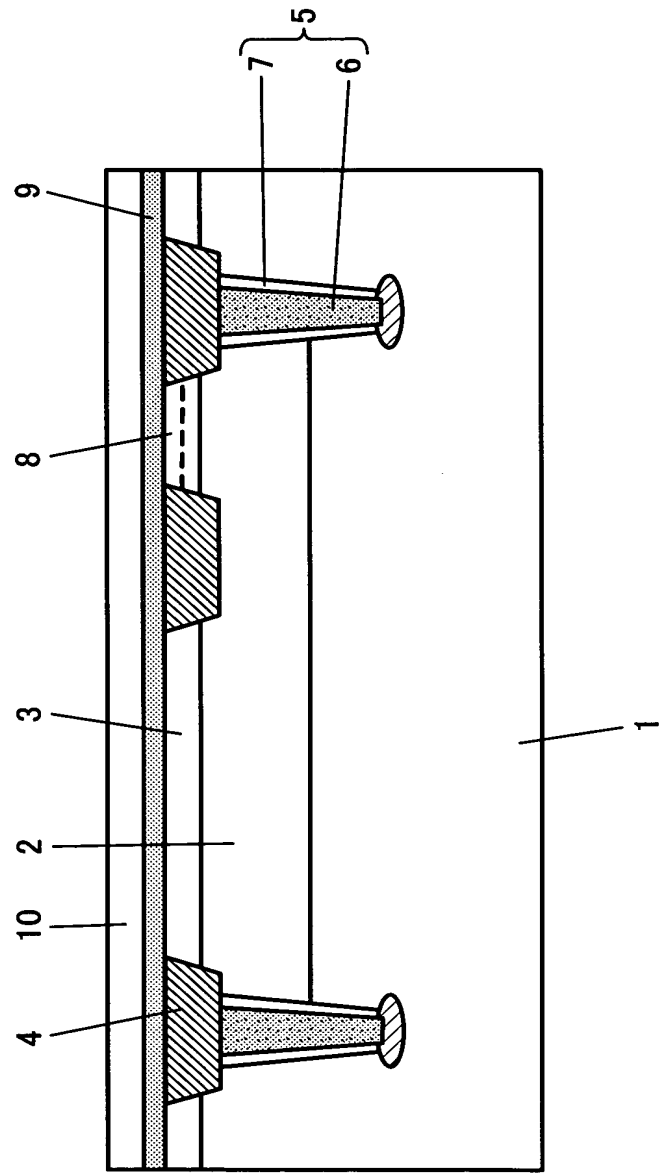


FIG. 4



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FIG. 5



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FIG. 6

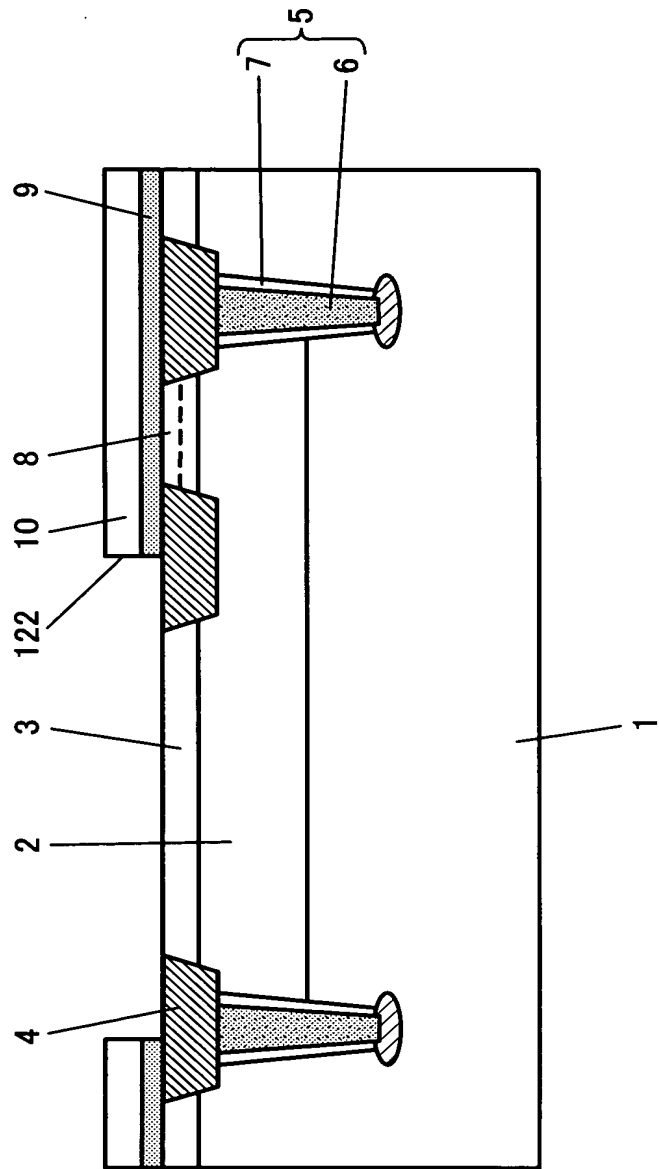


FIG. 7

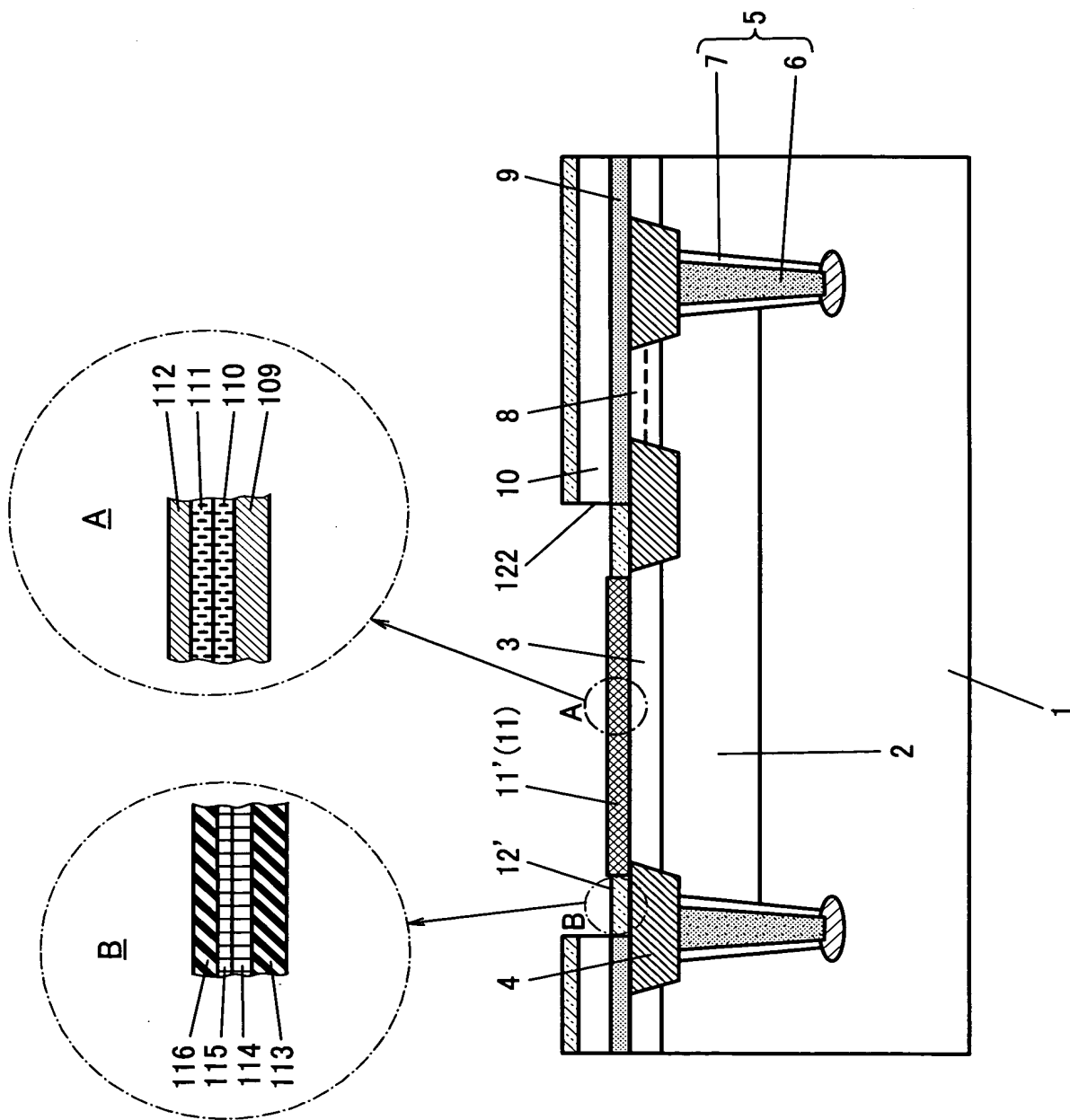
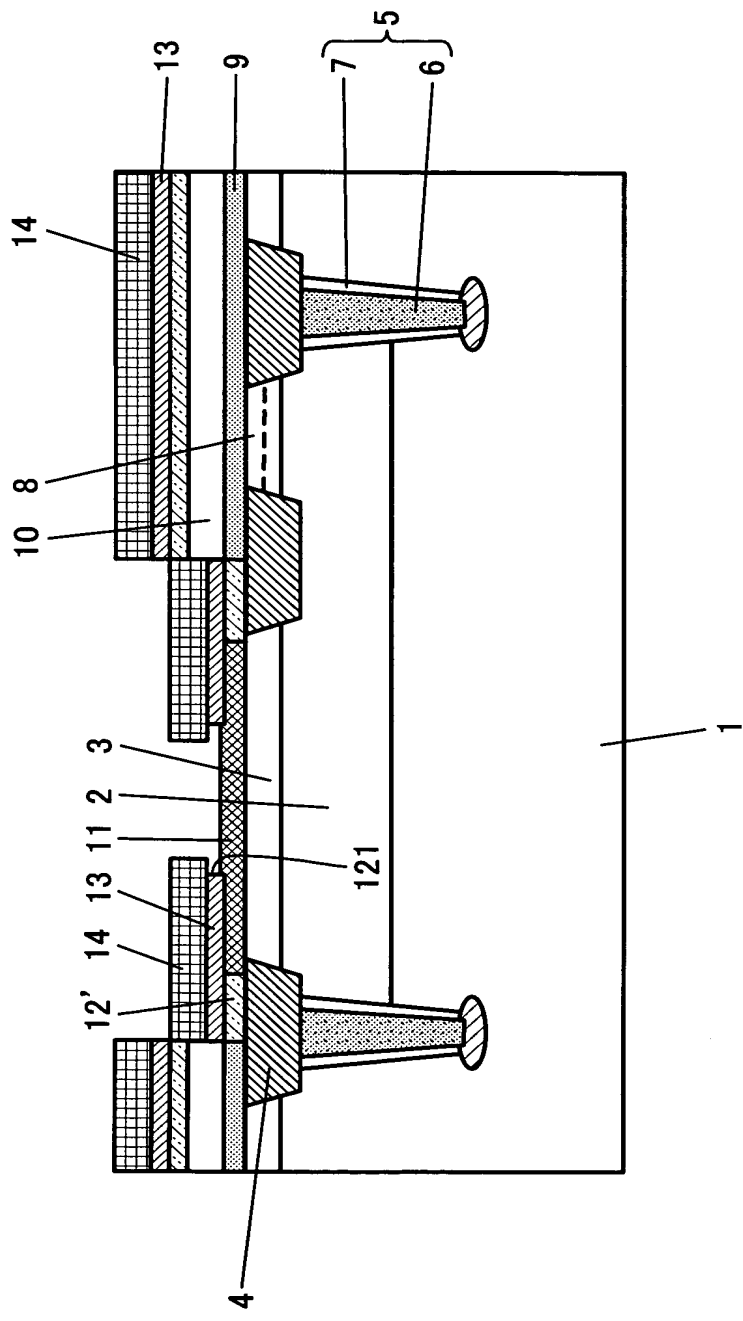


FIG. 8



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FIG. 9

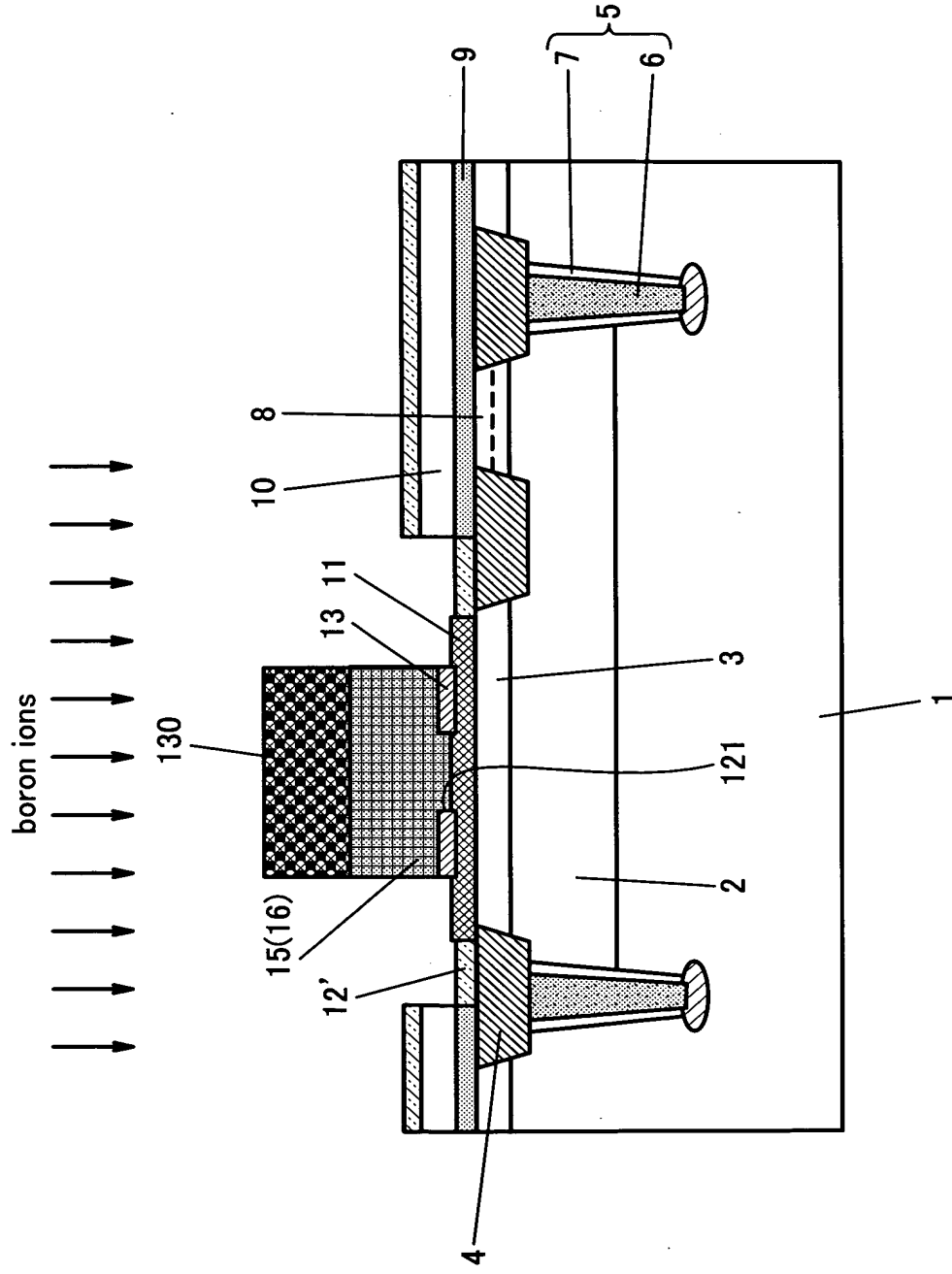
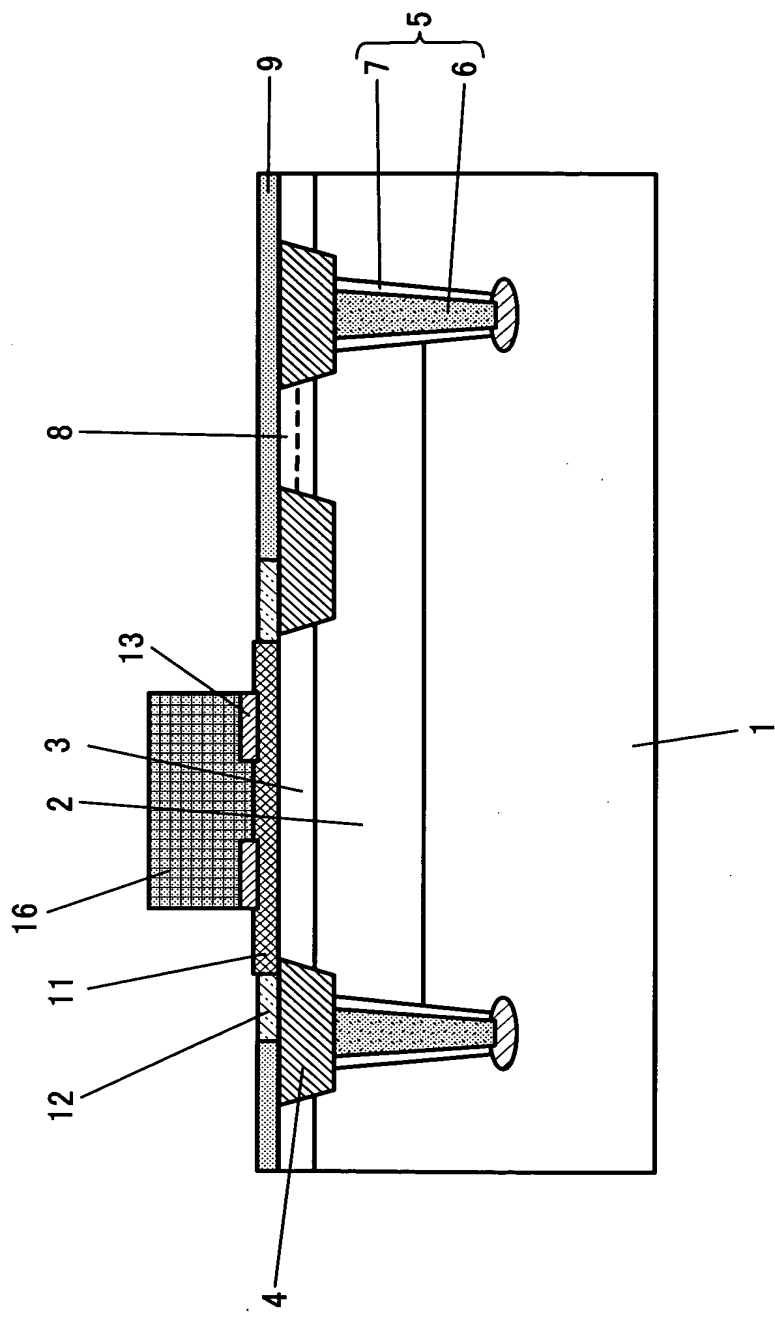
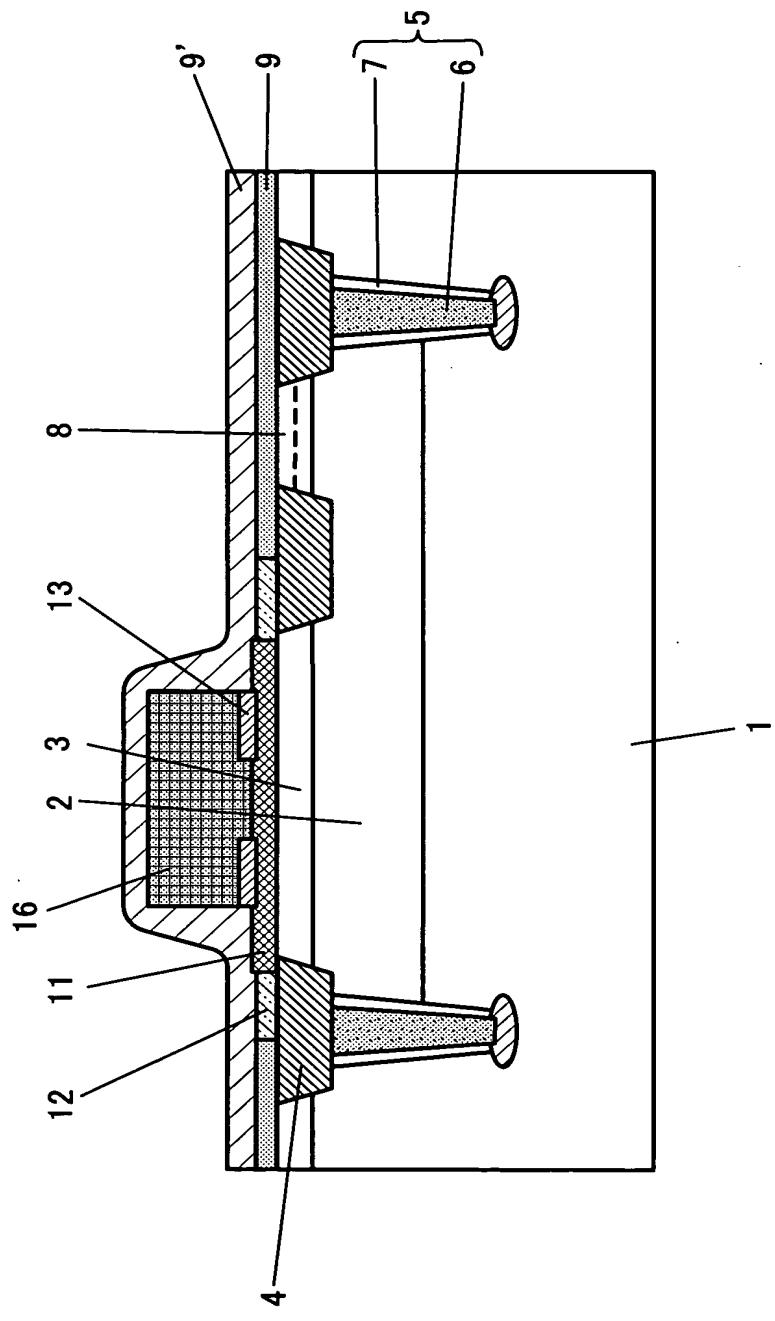


FIG. 10



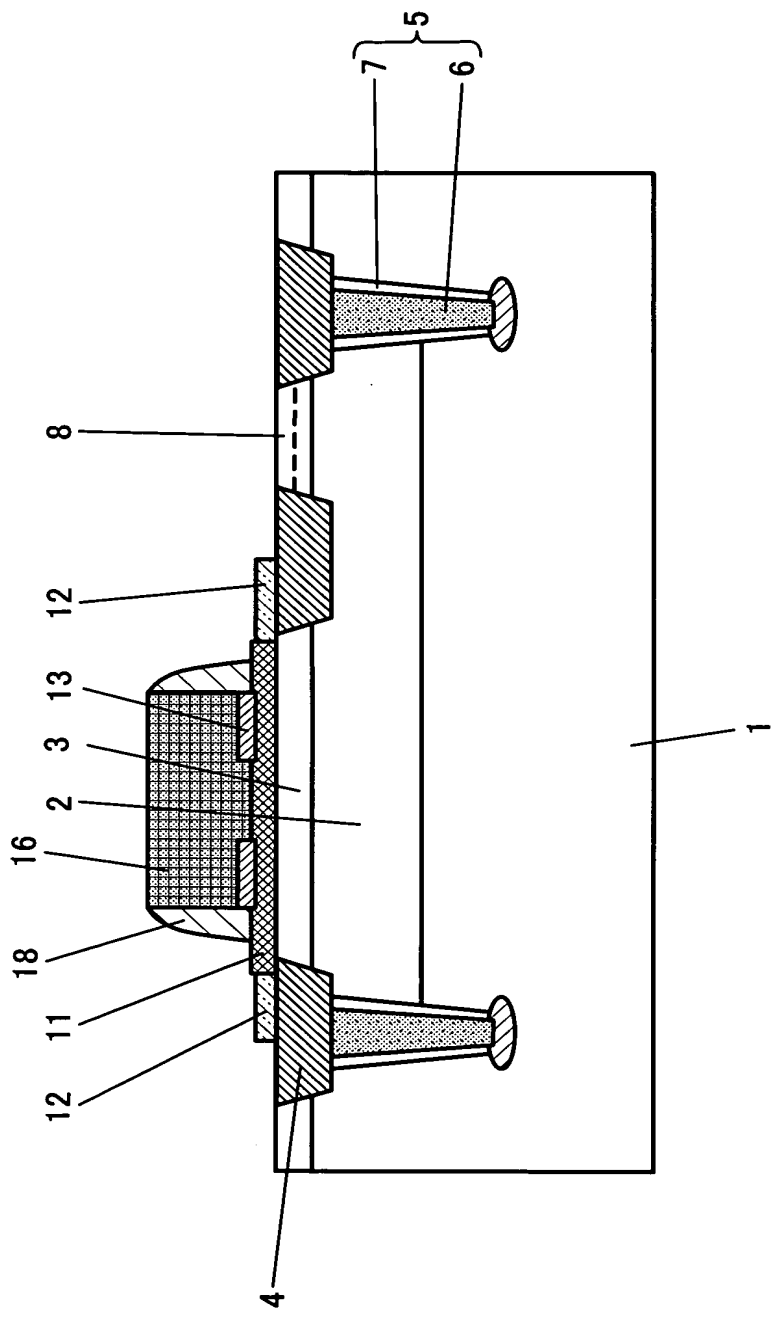
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FIG. 11



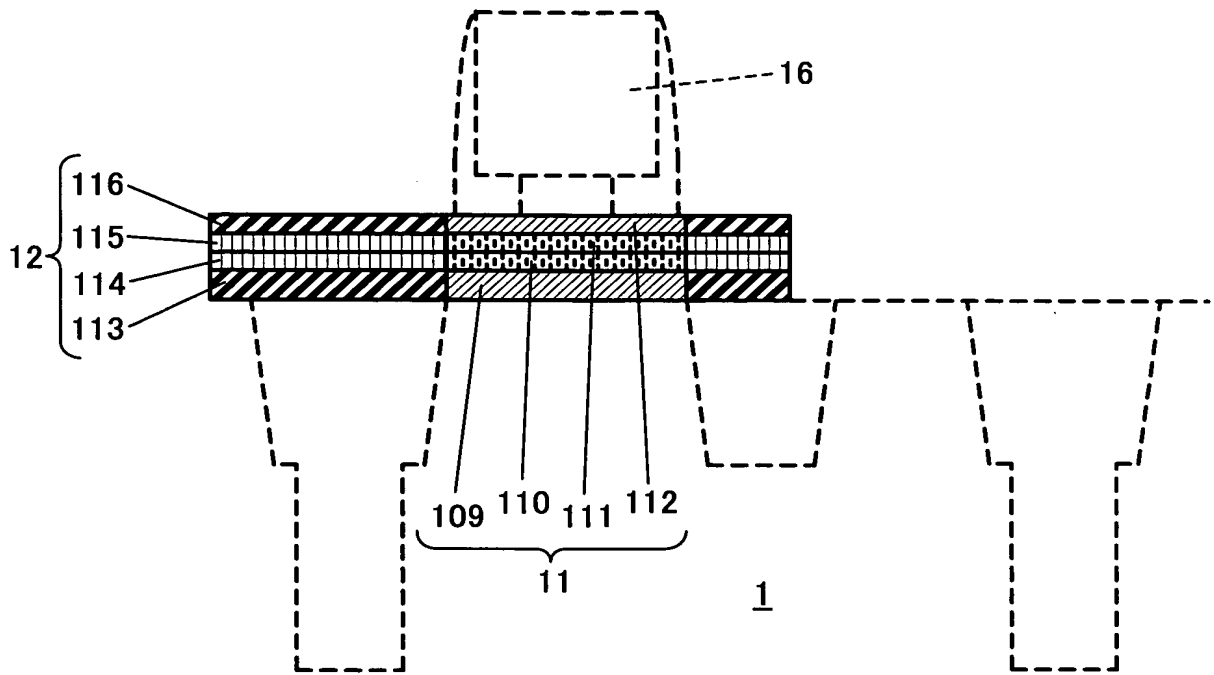
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FIG. 12

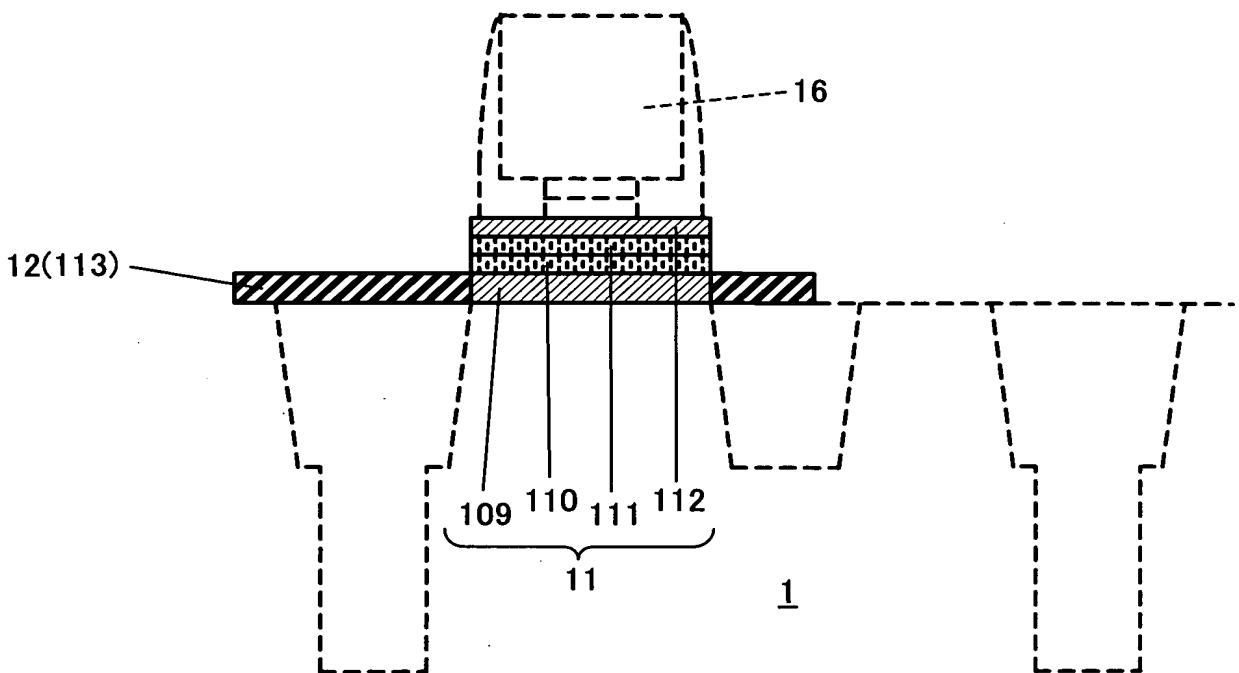


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FIG. 13



(a)



(b)

FIG. 14

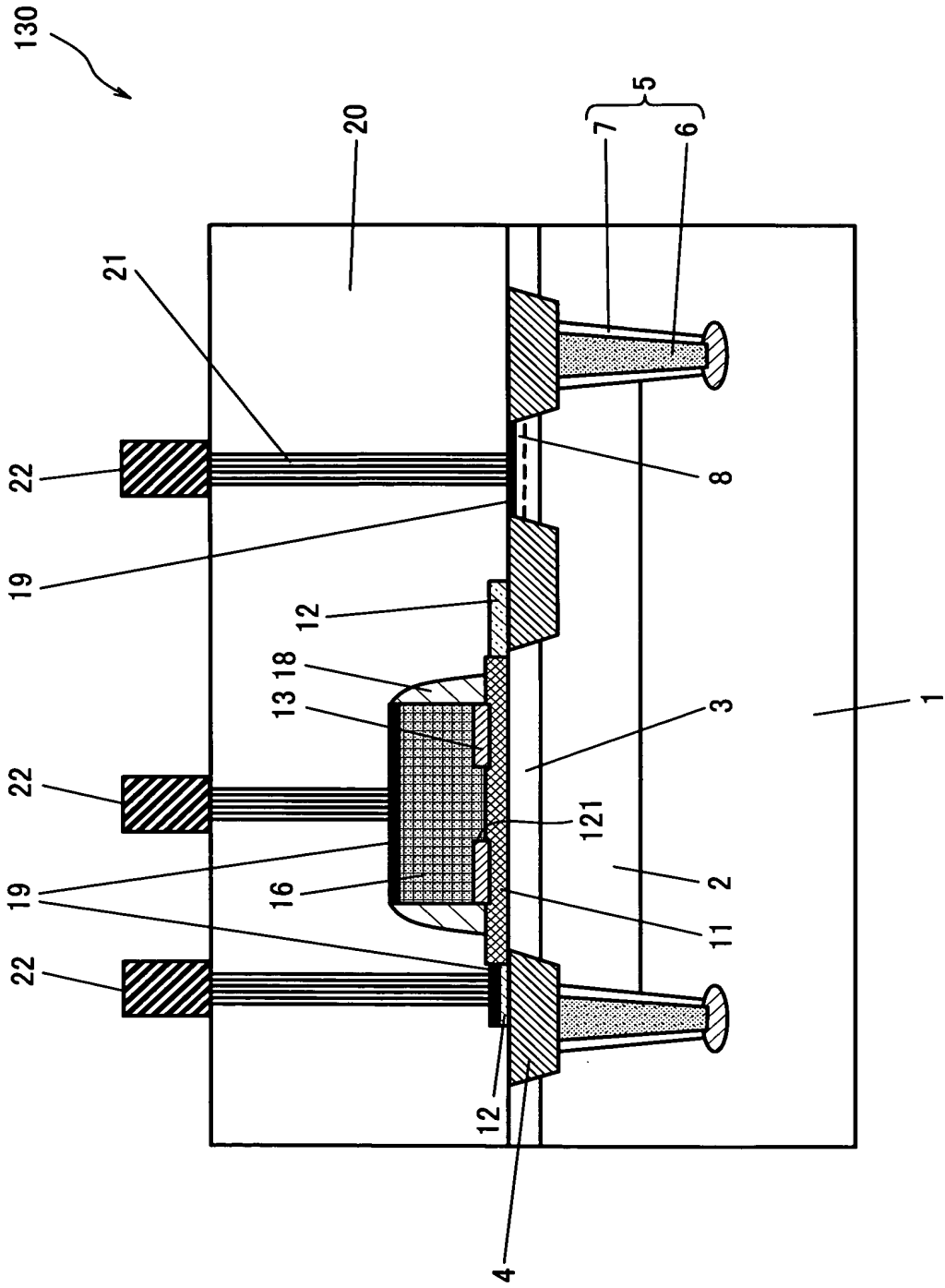


FIG. 15

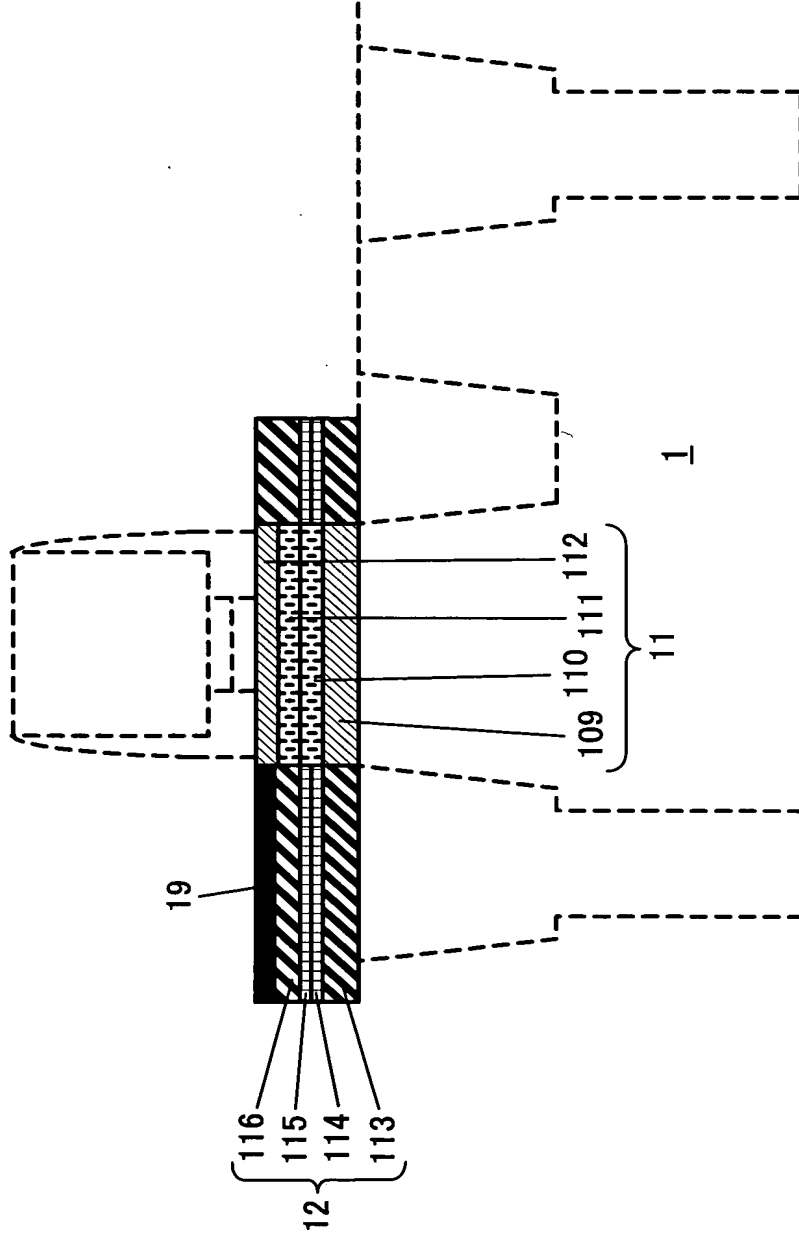


FIG. 16

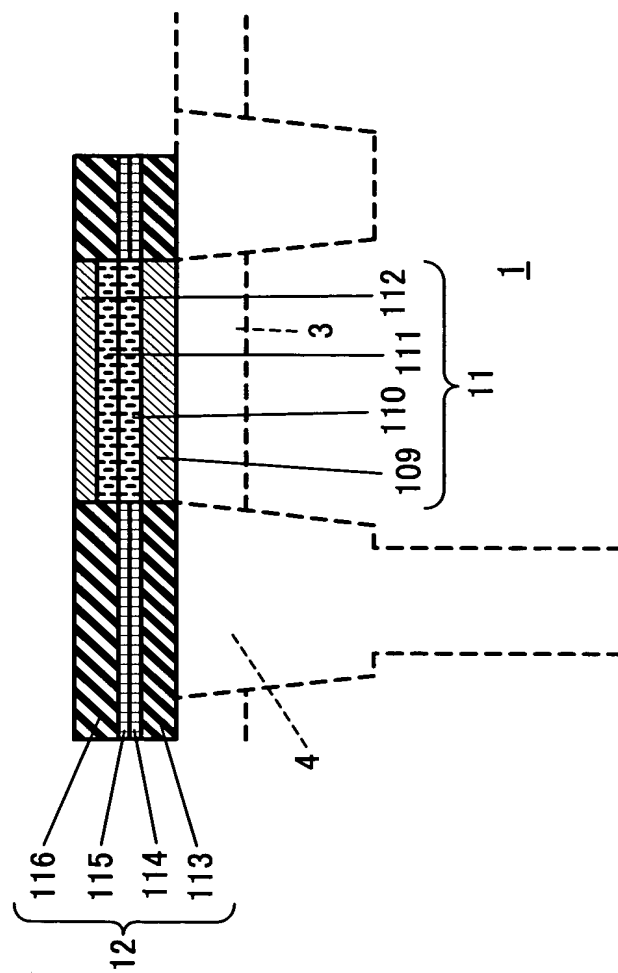


FIG. 17

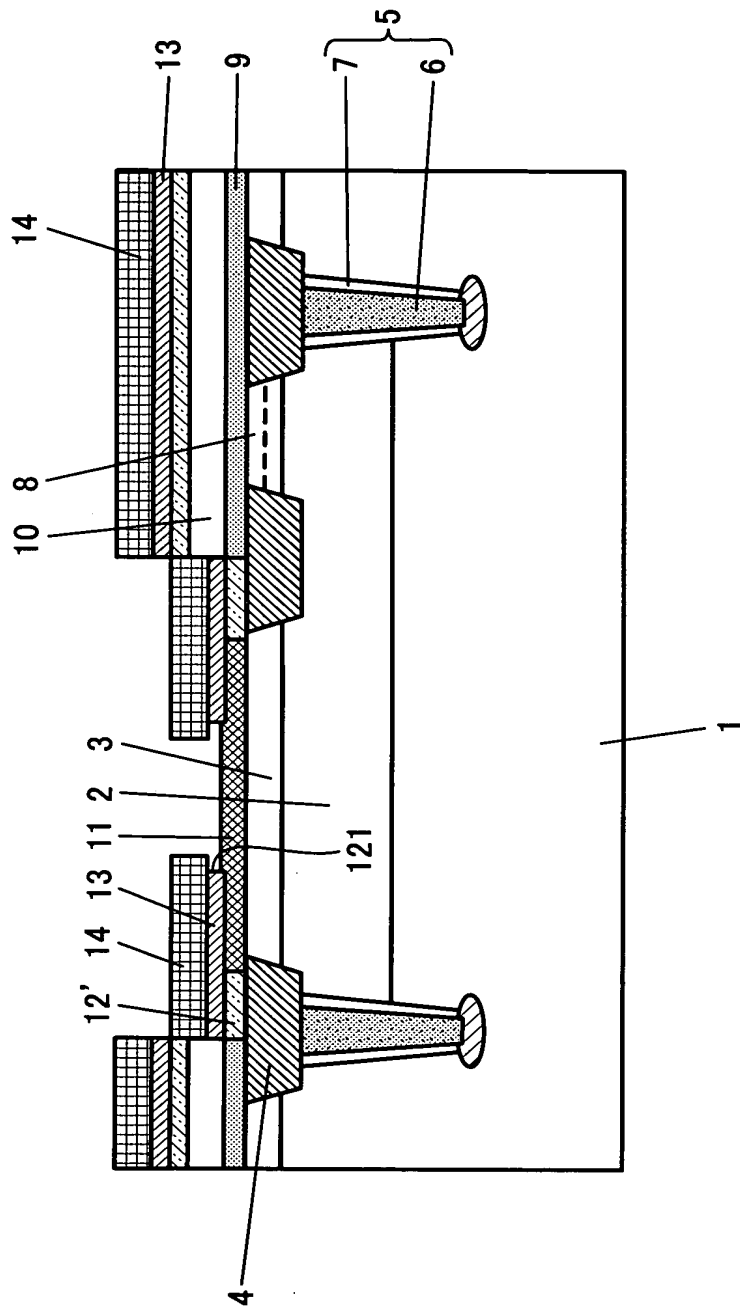
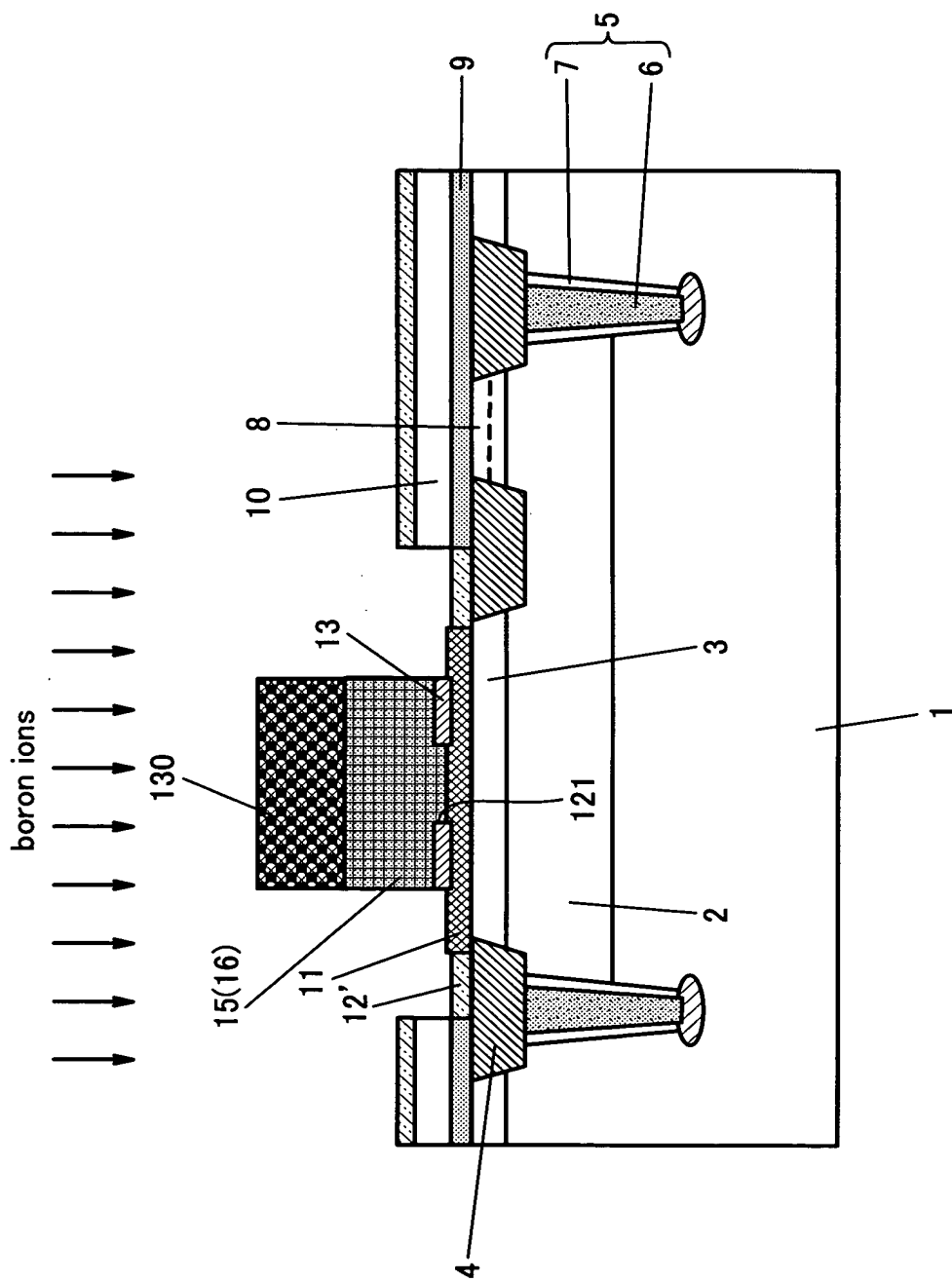
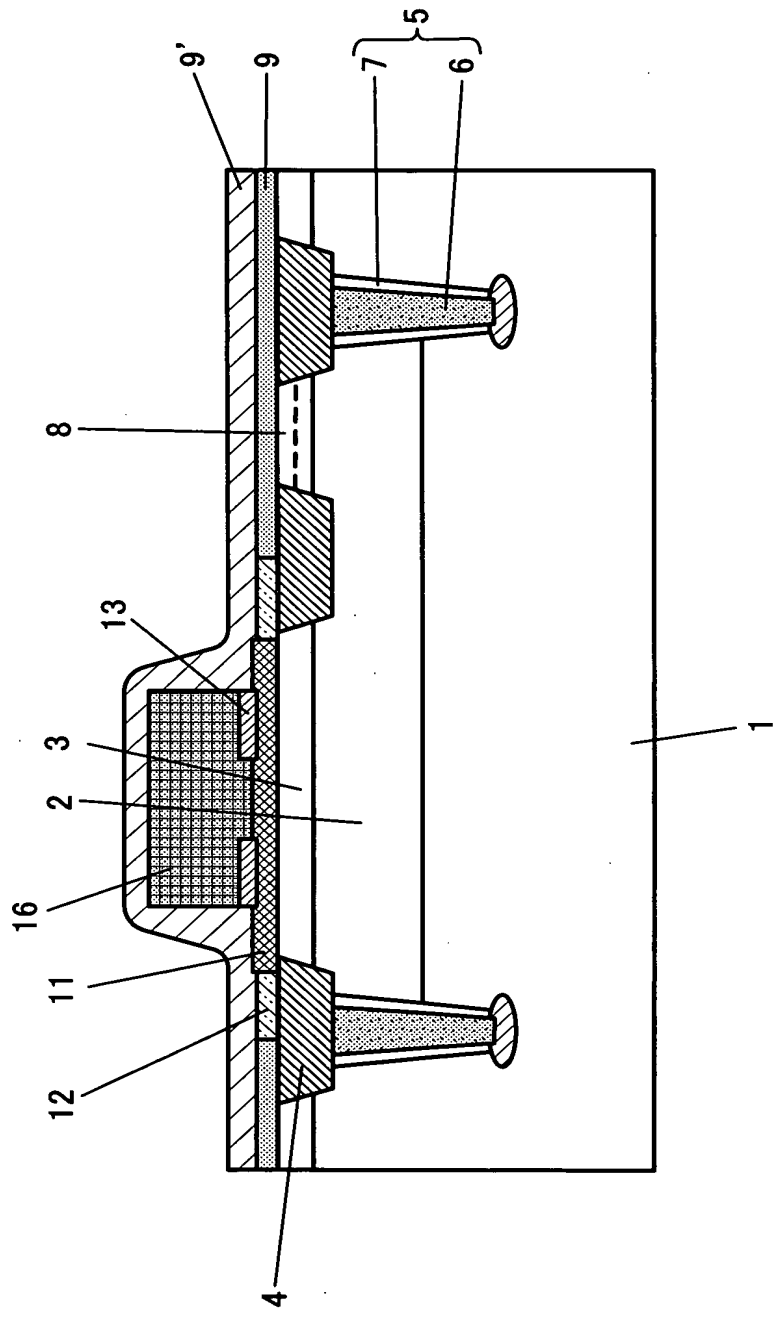


FIG. 18



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FIG. 19



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FIG. 21

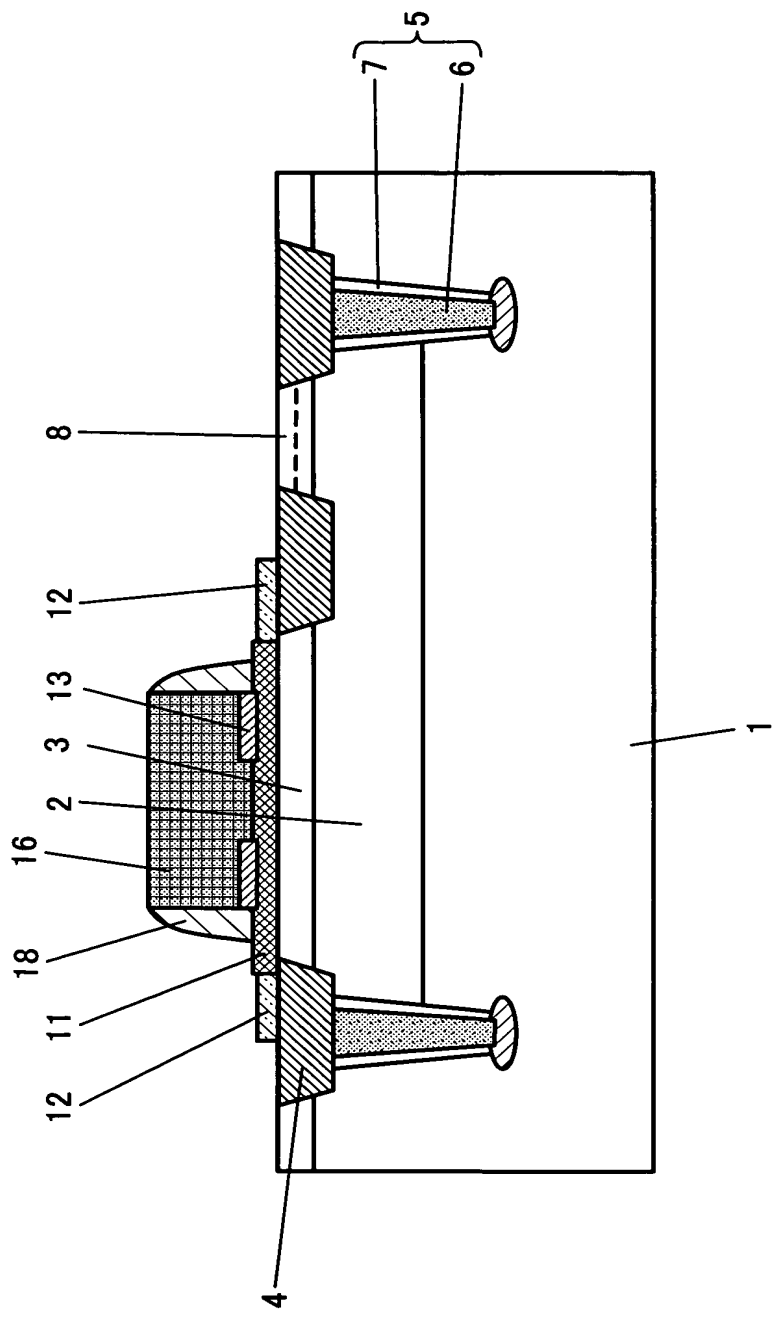


FIG. 22

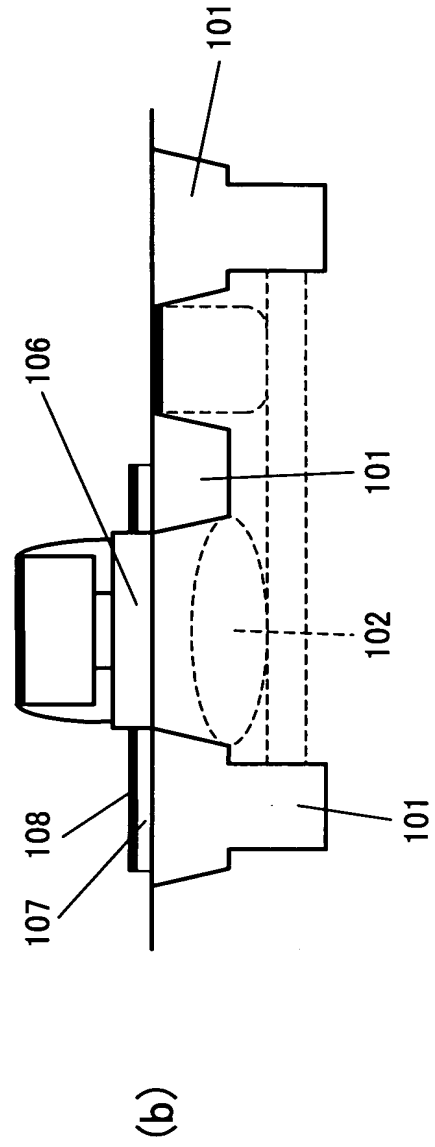
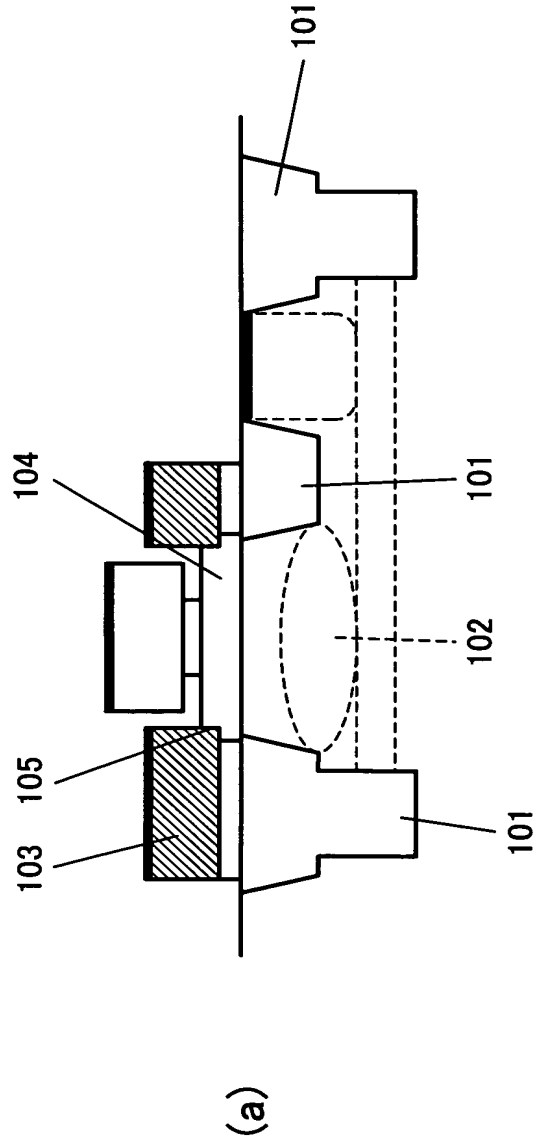


FIG. 23

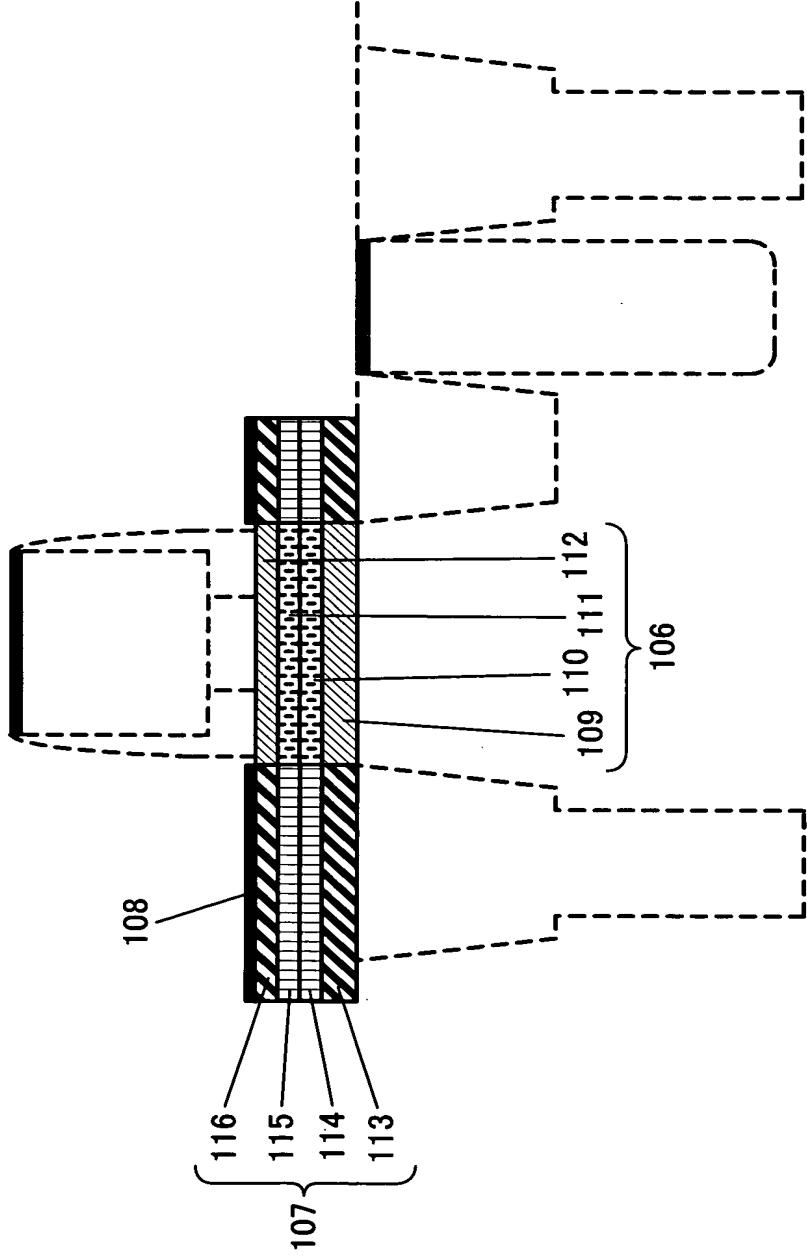


FIG. 24

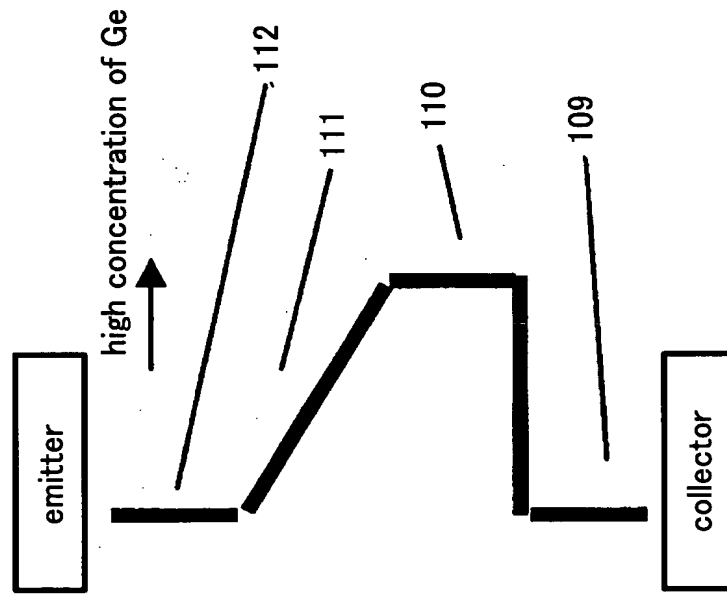


FIG. 25

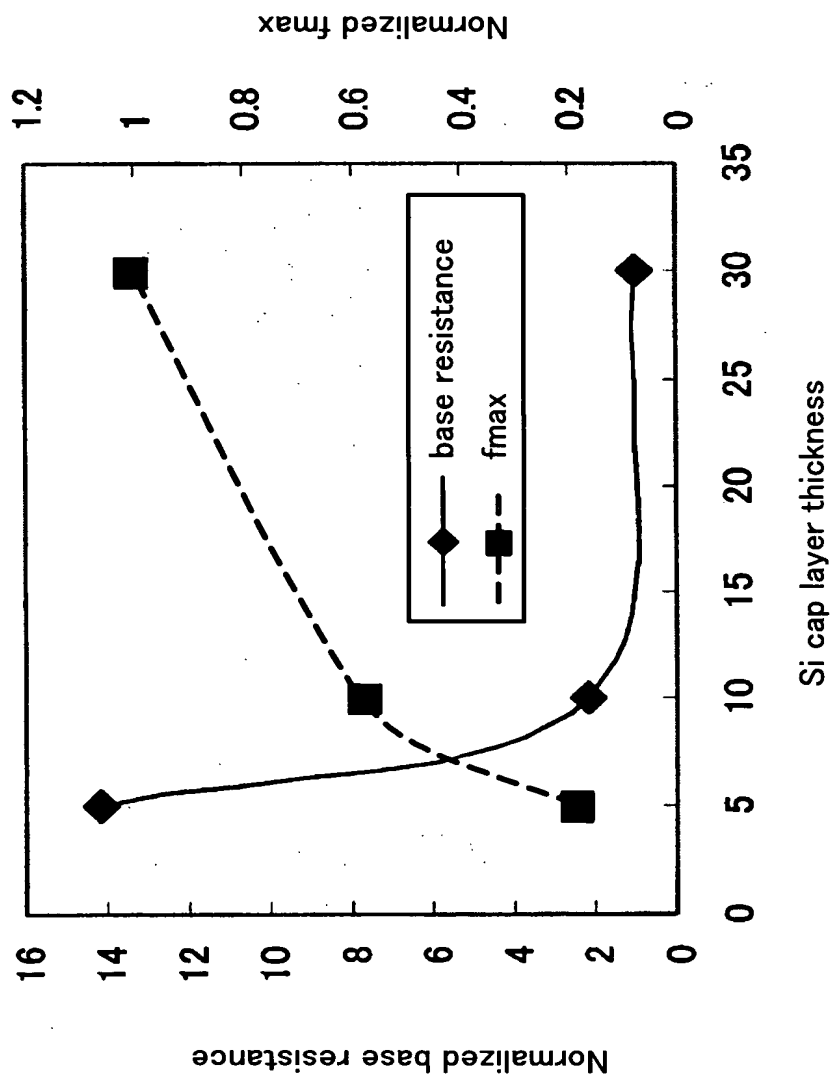


FIG. 26

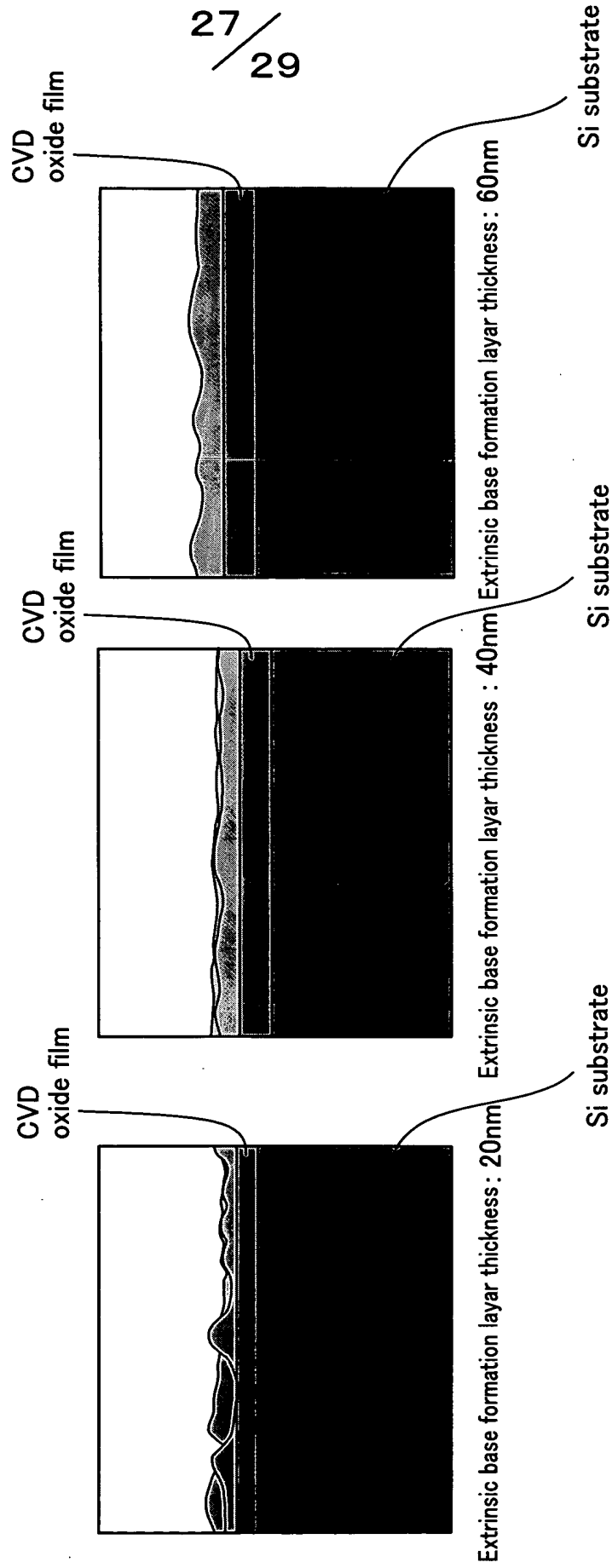
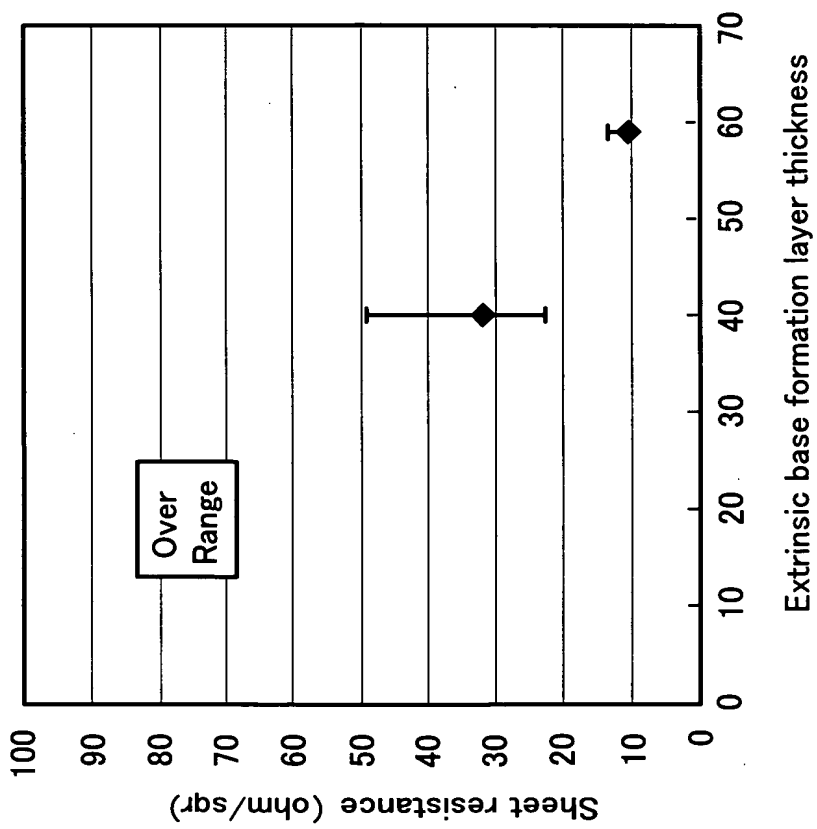


FIG. 27



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FIG. 28

Reference Number Table

1	Si substrate
2	subcollector region
3	Si monocrystal layer
4	shallow trench
5	deep trench
6	non-dope polysilicon layer
7、9、9'、13	silicon oxide layer
8	collector extract layer
10、14	polysilicon film
11	intrinsic base region
11'	epitaxial SiGe layer
12	extrinsic base region
12'	polySiGe layer
15	polysilicon layer
16	emitter electrode
18	side wall
19	Co silicide layer
20	interlayer dielectric
21	W plug
22	metal wiring
109	Si buffer layer
110	non-dope SiGe spacer layer
111	B-dope SiGe graded base layer
112	Si cap layer
113	extrinsic base formation layer
114	the second layer
115	the third layer
116	the fourth layer
121	opening
122	collector opening
130	resist